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ASSESSING POLYMERIC NANOCOMPOSITES AND ADVANCED COOLING TECHNIQUES FOR THERMAL MANAGEMENT OF NEXT-GENERATION POWER ELECTRONICS

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by

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Abstract

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The field of power electronics devices has seen two significant trends in recent years: rapid miniaturization of devices and the replacement of silicon-based devices with wide bandgap semiconductor materials-based devices (Silicon Carbide (SiC), Gallium Nitride (GaN)). The end result of these advancements are devices that need advanced cooling technologies to dissipate ultrahigh high and concentrated heat loads. Multiple advanced thermal management solutions such as liquid cooling, jet, and spray impingement have been proposed as potential solutions. The present dissertation quantifies the benefits of key advanced cooling techniques for thermal management of power electronics packages. An analytical modeling framework based on a thermal resistance circuit has been utilized to estimate the maximum heat flux that can be dissipated from a power electronics package, and the junction temperatures at varying levels of power dissipation. Analysis was conducted for heat sinks made of copper (k=400 W/mK) and a polymer (k=20 W/mK).

The developed modeling framework takes into account heat spreading in both lateral directions while capturing the influence of material properties on the spreading angle. The model can, therefore, be considered to capture 3D effects as well. Additionally, 3D Finite Element Analysis (FEA) simulations have been carried out to compare with the findings of the analytical model. This dissertation also studies the influence of polymeric encapsulants of varying thermal conductivities on the resulting temperature distributions in the package via steady 2D coupled electro-thermal simulations. Overall, the methodology and results presented in this dissertation provide insights for selecting optimal combinations of thermal management technologies and advanced polymeric materials, based on the heat dissipation requirements of power electronics packages.

Table of Contents

List of Tables

List of Figures

CHAPTER 1: INTRODUCTION

1.1 Power electronics

Power electronics devices include all of the switching-related solid-state electronic circuits used for converting and controlling the flow of electrical energy. Such components play a key role in the generation-conversion-storage-distribution cycle of electrical energy, which accounts for 40% of the worldwide energy generation [1]. Power electronics devices with origins as far back as the early 1900s have gradually made their way into a wide spectrum of applications such as: handheld devices such as mobile phones; household devices such as air-conditioners, refrigerators, personal computers, washing machines; industrial applications such as high voltage direct current (HVDC) transmission, electric motors, telecommunications systems, etc. Key enablers of such power electronics devices are solid-state semiconductors that help control and convert electric power with high efficiency.

Silicon (Si), being a widely available element, has been the traditional material of choice for semiconductor chips. However, it faces constraints due to lower operating temperature ratings, breakdown voltages, and switching frequencies [2]–[4]. Additionally, the performance of Si-based devices is reaching its limits, as dictated by the fundamental properties of the material. Silicon carbide (SiC) and Gallium Nitride (GaN) have emerged as popular alternatives to silicon. SiC and GaN are wide band gap (WBG) materials, and have advantages over Si with respect to optimal tradeoffs between their material properties, commercial availability of raw materials and well established technological processes[5]. In general, WBG materials are of high interest for use in high power switching devices. While device technology has gradually transitioned from Si to WBG materials, the packaging industry has relatively higher inertia and hence remains in a silicon or a pre-

WBG phase due to a number of factors such as cost or lack of significantly better packaging solutions[6]. Further advancements in power electronics semiconductor technology therefore greatly hinges on the development of innovative packaging solutions to harness the benefits of WBG semiconductors.

1.2 Thermal management of power electronics

Rapid miniaturization of power electronic devices, accompanied by increasing power dissipation has resulted in a steady rise in heat densities in such devices. Nearly 60% of the failures encountered in power electronics packages can be attributed to inadequate thermal management, with the failure rate doubling for every 10 ^{o}C rise in the operating temperature [7], [8]. While WBG materials can operate at higher temperatures, have a higher breakdown voltage and can withstand higher current densities when compared to their Si counterparts; thermal management still remains critical to device and package reliabilty.

Many recent thermal management solutions involve advanced single and two-phase cooling technologies that remove the heat via a heat sink connected to the package using a fluid or air as the coolant. While air-cooling is always attractive from a simplicity and ease-of-implementation standpoint, it imposes stringent limitations on the heat dissipation capacity owing to poor heat transfer coefficients associated with air. Liquid cooling becomes essential to realize high power compact packages. Even within liquid cooling, there are multiple technologies and options including single versus two-phase cooling and flow (in channels) versus liquid impact cooling (jets, sprays). Besides, there are multiple options for working fluids (water, dielectric fluids). While these cooling technologies can significantly augment the heat dissipation capability, they necessitate pumping power and result in increased complexities (associated with heat-sink design, fabrication), hermeticity

requirements, and higher costs. Nevertheless, the electronics cooling community is unanimous that next-generation power electronics packages will necessarily require liquid cooling to meet thermal management challenges while shrinking package sizes.

Most of the advanced cooling solutions primarily focus only on the downward pathway for heat removal via a heat sink (usually metallic) connected to the bottom of the case. The electronics package encasing, which represents the shortest path from the heat-generating point (chip) to the universal heat sink (atmosphere), is commonly neglected from a thermal standpoint. The package used to encase the chip and the solid-state electronics protects its components from mechanical damage, chemical corrosion, moisture in the atmosphere, radiation, etc. Recent advancements in semiconductor technology have necessitated a concurrent growth in corresponding packaging technologies to account for the growing electrical, mechanical and thermal constraints. Notably, many materials in existing packages have very poor thermal conductivity (< 1 W/mK), thereby insulating or cutting off the vertically upward pathway for heat removal. Furthermore, any attempts towards enhancing the thermal conductivity leads to a decrease in electrical conductivity, which is an important parameter for the safe operation of the device. While Si-based semiconductor technologies are slowly being replaced by the advanced and improved SiC and GaN-based WBG technology, the packages encasing these semiconductors still remain in the pre-WBG era. This severely limits the potential benefits of WBG devices. It is clear that Si-based packages will be unable to meet the high thermal, electrical and mechanical requirements of WBG devices and represent a significant technological hurdle.

1.3 Use of polymers in power electronics packaging

Polymers are widely utilized as packaging and insulating materials in power electronic packages due to their ease of electrically insulating nature, manufacturability, low cost, tunable properties via modification of composite blends, low dielectric constant, etc. [9]. Such polymers are meant to serve multifunctional (thermal, mechanical, electrical) requirements. While existing polymers can meet the electrical and mechanical requirements to a reasonable extent, they perform rather poorly from a thermal standpoint. In order to identify areas for improvement, it is important to understand various ways in which polymers are used in power electronics packaging. Presently, polymers in power electronic packages are primarily used in one of the following forms[10]:

i. Conformal coatings

A thin layer of polymer is sprayed on to the printed circuit board (PCB) to conform to its contours thus protecting against humidity, chemicals, dust, and temperature extremes. In addition to environmental protection, such coatings provide electrical insulation for operating components thus enabling them to operate at higher voltage gradients [11]. Since conformal coatings are thin with typical thicknesses in the 25-250 μm range. Electrical circuitry can be reworked at a later stage, unlike thick potting compounds that exclude the possibility of reworking at a later stage. Epoxies, silicones, polyurethanes, and acrylics have been commonly employed to protect wiring assemblies from moisture and chemically-induced corrosion. Conformal coatings are primarily used in harsh operating condition-based environments such as military, aerospace, marine industries but are also being used in domestic appliances and mobile electronics. Typical coating methods include brush coating, dip coating, spray coating, spin coating, vapor

deposition, conformal coat dipping, etc. Such coatings typically have low hygroscopic absorption to prevent corrosion of metallic parts, good adhesion with the substrate components, high dielectric strength to prevent breakdown, and a matching coefficient of thermal expansion (CTE) with the base component to minimize thermal stresses. While acrylic, polyurethane, epoxies can be used for low (165 ^{o}C) to moderate (200 ^{o}C) temperature applications, silicones, polyimides are typically used for electronics applications at higher temperatures (>200 ^{o}C).

ii. Potting encapsulation

The primary purpose of a potting encapsulation is protecting the base circuit and interconnections from moisture, electrical breakdown, mobile ion contaminants, ultraviolet-visible and alpha particle radiation, and unfavorable environmental conditions such as unforeseen excursions in temperature and moisture[12], [13]. The reliability of the encapsulated device primarily depends on three important properties of the encapsulant- the coefficient of thermal expansion (CTE), modulus of elasticity (E), and dielectric breakdown strength. The cyclical thermal stresses resulting in some regions of the package, especially around wire bonds, can be alleviated by the use of an encapsulant with CTE matching those of the wire and substrate. Furthermore, such encapsulants should have a high moisture and contaminant barrier ability to prevent diffusion into the substrate, low dielectric constant, high voltage breakdown strength, excellent adhesion and ease of processability. Cavity filling and saturation and coating processes are commonly used as package encapsulating techniques. Commonly used encapsulants include polyurethanes for low temperature (<165 ^{o}C) applications, epoxies for mid-temperature (<200 ^{o}C) applications, and silicone-based gels, benzocyclobutane

(BCB), polyimides and elastomers for high-temperature applications (up to 300 ^{o}C).

iii. Underfillings

Underfills are primarily used to alleviate the thermo-mechanical stresses arising due to CTE mismatch between different materials in the package, specifically the area around the solder balls between the chip and the direct bonded copper (DBC) substrate. Favorable properties include a CTE matching those of different components (20-30 ppm), a high glass transition temperature, low moisture absorption, good adhesion, low viscosity for ease of processing. Such underfills are usually applied along the edge of the chip while it gets pulled into the gap between the chip and DBC due to capillary effect. Typically, filler materials are added to a base polymer matrix to produce nanocomposites with tunable CTE values. However, the addition of such filler materials usually increases the viscosity which gives rise to processability-related issues.

Based on the above mentioned applications, recommended properties [10] for polymer/nanocomposites are outlined in Figure 1.

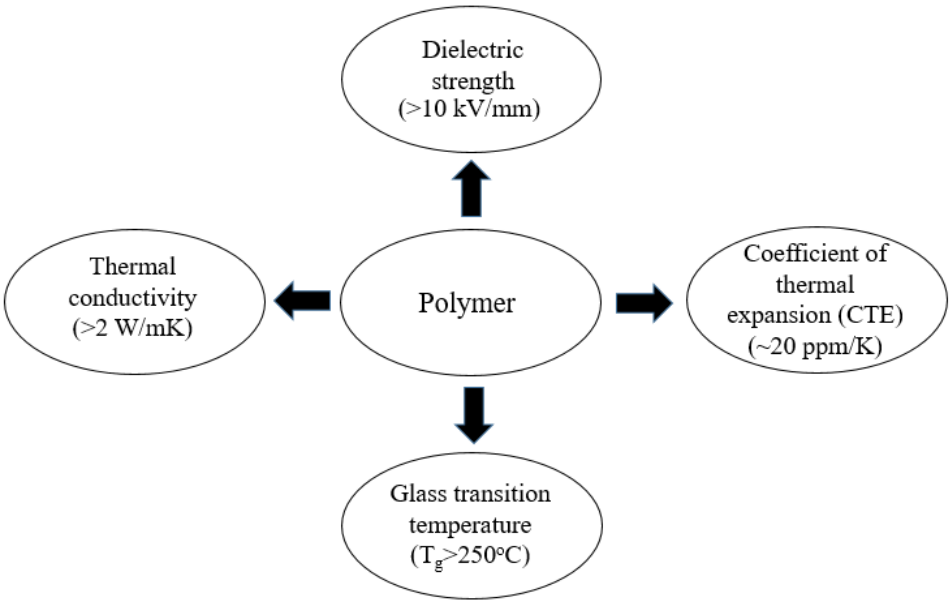

Figure 1. Recommended properties of polymers for use in power electronics encapsulation applications [10]**.**

While polymeric encapsulants serve multiple purposes in a package (protection from the environment, mechanical shocks, etc.), they are also prominently located in the heat flow pathway from the chip junction (highest temperature point in the thermal circuit) to ambient air (to which heat is eventually rejected). The use of novel high thermal conductivity polymers can make a significant difference to the overall thermal performance of the package. It is noted that the polymers used in traditional encapsulation have a thermal conductivity of ~ 0.2 W/mK, which is just ten times higher than air and 2000 times lower than copper, which is a commonly used heat sink material. Over the past two decades, there has been significant progress in developing novel polymer composite materials with much higher thermal conductivities, by adding high thermal conductivity filler materials (boron nitride, aluminum oxide, silicon carbide, aluminum nitride, etc.) to a base polymer [10], [14]. While such filler materials significantly augment the thermal conductivity of the base polymer matrix, they also affect the mechanical and electrical properties such as CTE,

dielectric strength, etc. Table 1 summarizes the key developments in efforts aimed at improving thermal properties of polymeric nanocomposites by adding filler particles with a high thermal conductivity for use in power electronic applications. Polymeric materials with thermal conductivities of O(1) W/mK are commercially available and materials with O(10-100) W/mK are in the research phase [9], [15], [16].

While such materials have been developed primarily for use as advanced encapsulants, they can also be used to fabricate heat sinks. There has been notable recent research on the development of polymeric heat sinks [17]. While polymeric heat sinks will not offer the thermal performance associated with copper (thermal conductivity 350 W/mK) or aluminum (thermal conductivity 150 W/mK) heat sinks, they offer other significant advantages such as higher heat dissipation to weight ratios, ease in fabrication, and corrosion resistance [17]. This dissertation studies the impact of high thermal conductivity polymeric heat sinks on thermal management of power electronics.

Table 1. Reported thermal conductivities of polymeric composites

#	Polymer matrix	Filler material	Thermal conductivity of composite (W/mK)	Ref
1	Polybenzoxazine	h-BN	32.5	[18]
2	Epoxy	Ag-BN	23.1	[19]
3	Cellulose	h-BN	22.9	[20]
4	Cellulose nanofibers	BNNTs	21.4	[21]
5	Cellulose nanofibers	BNNTs	20.9	[22]
6	Epoxy	BN	13.5	[23]
7	Polyvinylidene fuoride	AlN	11.5	[24]
8	Epoxy	AlN	11	[25]
9	Polyimide	AlN+ h-BN	9.3	[26]
10	Epoxy	AlN	8.2	[27]

1.4 Outline of dissertation

Chapter 2 presents an analytical modeling framework (based on a thermal resistance network) to analyze the influence of using advanced cooling technologies and polymeric heat sinks on the thermal performance of an Insulated gate-bipolar transistor (IGBT) package. In this study, the convective heat transfer coefficients for various cooling technologies are evaluated using well-established correlations. The maximum heat flux that can be dissipated for Si and SiC electronics is estimated. The resulting junction temperatures for various levels of heat dissipation for different cooling technologies, are also estimated.

Chapter 3 outlines a brief study on using 3D Finite Element Analysis (FEA) simulations to evaluate the thermal performance of the package and compare the obtained results with the analytical model detailed in Chapter 2. Additionally, simple, coupled 2-D electro-thermal simulations are carried out to outline the influence of the thermal conductivity of polymeric encapsulants on the temperature distribution inside the package.

CHAPTER 2: ANALYTICAL THERMAL MODELLING OF POWER ELECTRONICS PACKAGE

[1]This chapter assesses the thermal performance of advanced liquid cooling techniques, and the use of polymeric heat sinks on a commercially available insulated-gate bipolar transistor (IGBT) package. An analytical modeling framework, based on a thermal resistance network, is developed and utilized to assess and compare various thermal management options. While the thermal resistance-based model is purely analytical in nature, it does address important complexities associated with heat flow in packages via the use of a sub-model to account for thermal spreading. Simulations are conducted for power electronics packages based on silicon as well as silicon carbide electronics, to quantify the maximum allowable heat flux, subject to the junction temperature limits. It is noted that such models can be used for a first-order assessment of promising cooling technologies and materials, with the view of identifying candidates for further detailed analysis.

2.1 Modelling framework to evaluate advanced cooling technologies

2.1.1 Approach underlying current simulations

A thermal resistance network-based model is used to predict the maximum allowable heat flux for the thermal management solution being analyzed. The maximum

[1] Chapter 2 is based on a previously published article by the author. The author conducted all analysis. Acharya P.V., Bahadur V., Hebner R., Ouroua A., Strank S., Assessing the performance of advanced cooling techniques on thermal management of next-generation power electronics, Proceedings of the International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems (IPack 2019), Anaheim, CA, USA

allowable junction temperature is fixed as 125 ^{o}C for Si-based electronics and 200 ^{o}C for SiC-based electronics (WBG material)[28]. Variable angle model (VAM) is used to estimate the thermal resistance of every layer of the IGBT module until the baseplate. The thermal resistance of the heat sinks are estimated from heat transfer coefficients, which are evaluated using well-established correlations. It is noted that this model does not accurately capture the intricacies of heat transfer in an actual package, and will not yield high fidelity temperature predictions obtainable from 3D numerical solutions of the governing equations. This model is intended to be a tool for a rapid, first-order assessment of various materials and cooling technologies, and for related parametric studies. It is also noted that this thermal resistance network is related to Foster and Cauer network modeling [29], [30], and can be extended to include thermal capacitances for transient analysis.

2.1.2 Brief description of power electronics package modeled in the present work

Geometric parameters used in the present model were extracted from details of a 1700V/75A IGBT module (SKM75GB12T4, made by Semikron) [31]. A schematic of the package cross-section is depicted in Figure 2. Material properties and dimensions of individual layers used to estimate the thermal resistances are presented in Table 2.

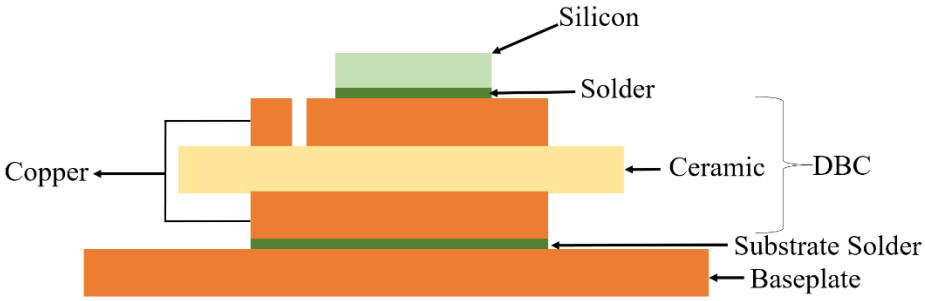

Figure 2. Schematic of the IGBT package modeled in the present study [6].

Table 2 Parameters of the package used in this study [23].

No.	Material layer	Thickness (mm)	Length (mm)	Width (mm)	Thermal conductivity (W/mK)
1	Silicon	0.15	7.24	6.9	153
2	Solder	0.12	7.24	6.9	66.8
3	Copper	0.3	28.5	25.8	401
4	Alumina	0.38	30.6	28	26
5	Copper	0.3	28.5	25.8	401
6	Solder	0.12	28.5	25.8	66.8
7	Baseplate	2.8	91.4	31.4	401

2.1.3 Variable Angle Model (VAM)

Heat spreading occurs in packages due to in-plane lateral conduction, when the cross-sectional area of the heat source is smaller than the subsequent layer through which heat diffuses. It is important to consider spreading resistance in packaging analysis, especially since devices are becoming more compact, while heat sinks are getting larger to dissipate higher quantities of heat. While several studies have examined heat spreading, the analytical infinite series-based estimates are difficult to implement due to the complexities associated with calculating the coefficient terms [32]–[35]. Usually, it is assumed that heat spreads at a constant 45º spreading angle from the power dissipating

source through various layers of a package with isotropic thermal conductivity[36], [37]. Such assumptions lead to inaccuracies in many situations, especially those involving multiple layers [38]. In reality, this value will depend on the thermal conductivities of different elements in the package. A closed-form expression of thermal resistance for circular, square and rectangular-based heat source geometries was derived for a single layer [37] which yielded results that matched the predictions of exact analytical solutions (infinite series summation) with less than 10% difference. Presently, we use the variable angle model (VAM) [38] which extends the approach described in [37] to include variable spreading in multiple layers. In this framework, the heat spreading angle in both the lateral dimensions is dependent on system geometry such as substrate and source dimensions and the boundary conditions at the interface (i.e., the thermal conductivity of the following layer).

Consider the geometry depicted in Figure 3, where a rectangular source element of dimensions ($2l_x$ by $2l_y$) is placed at the center of a rectangular substrate with dimensions ($2L_x$ by $2L_y$). The thermal resistance R_{th} for such a layer can be estimated as [38]:

$$R_{th} = \frac{1}{4k_i l_x}\left[\frac{1}{\left(\gamma_e.\tan\alpha - \tan\beta\right)}.\ln\frac{l_x + h.\tan\alpha}{l_x + h.\tan\beta/\gamma_e} + \frac{l_x.\left(w-h\right)}{{L_x}^2.\gamma_s}\right] \quad (1)$$

where:

$$\left(\tan\alpha\right)_i = \frac{w_i + \left[\frac{\rho_i}{1+\rho_i}\right].l_i}{w_i + \left[\frac{1}{1+\rho_i}\right].l_i}.\left(1 - \frac{l_i}{L_i}\right) \text{ ; h = min } \left(\frac{L_i - l_i}{\tan\alpha}, w_i\right) \quad (2)$$

$$\rho_i = \frac{k_i}{k_{i+1}}; \gamma_e = \frac{l_y}{l_x}; \quad \gamma_s = \frac{L_y}{L_x} \quad (3)$$

where, k_i denotes the thermal conductivity of layer i, α & β denote the spreading angles in x and y directions respectively, ρ_i is the ratio of the thermal conductivity of the layer i (k_i)

to that of the layer i+1 (k_{i+1}), and w_i is the thickness of layer i. The spreading angles in both the lateral and longitudinal directions can be obtained from the corresponding lengths in equation 2.

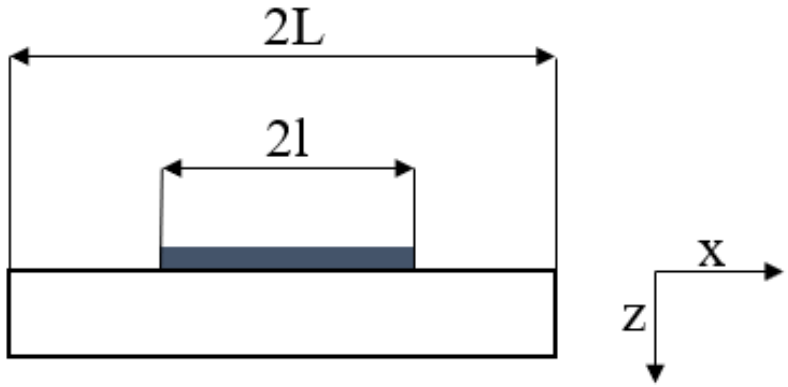

Figure 3. Schematic of the geometry used for the variable angle model calculations.

The analysis procedure is briefly described ahead. In order to evaluate the thermal resistance, the spreading angle and subsequently the thermal resistance for the present layer (i) was evaluated using the thermal conductivity of the next layer (i+1) as the boundary condition. The dimensions of the heat source were then projected onto the subsequent layer based on the spreading angle, to be used as the source dimensions for the next layer. This process was iteratively repeated until the bottom-most layer was reached. Resistances of the individual layers of the IGBT package, as calculated from this model were then used in a thermal resistance circuit. It is important to note that the variable angle spreading model captures the influence of heat spreading in both the lateral and longitudinal dimensions (based on material properties, structure, and boundary conditions). This approach can thus be considered to capture 3D effects as well.

2.2 Advanced cooling technologies assessed in this study

2.2.1 Air cooling: Finned heat sinks

Plate-fin heat sinks are among the most widely studied and employed thermal management solutions [39]–[41]. Such heat sinks, while being easy to manufacture, also offer benefits in terms of cost to thermal performance ratio. Plate-fin heat sinks employ either air or liquid cooling depending on the heat load.

In the current study, a plate-fin heat sink is studied with air and liquid cooling strategies to predict the maximum allowable heat flux that can be removed while maintaining the junctions below their rated temperatures. A schematic of such a plate-fin heat sink is depicted in Figure 4, and specific dimensions are tabulated in Table 3. This heat sink is thermally attached to the IGBT package shown in Figure 2 using a thermal interface material (TIM).

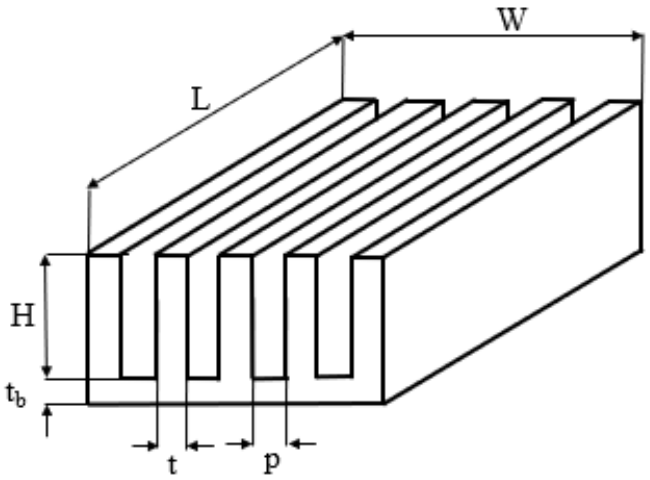

Figure 4. Schematic of the plate fin heat sink considered in the present study[39]

Table 3. Geometric parameters of the plate fin heat sink considered in the present study[39]

L (mm)	W (mm)	t_b (mm)	H (mm)	t (mm)	p (mm)
91.4	31.4	8.4	21.8	1	2.1

The parameters L, H, W, p, t_b, N and t denote the length, height, width, fin spacing, base thickness, number of fins, and thickness of the individual fins, respectively. We need to estimate the conductive and the convective resistances associated with airflow through the heat sink. The Nusselt number can be estimated using the following correlation [42]:

$$Nu = \left[\frac{1}{\left(0.5\,\mathrm{Re}_p^{*}\,\mathrm{Pr}\right)^3} + \frac{1}{\left(0.664\sqrt{\mathrm{Re}_p^{*}}\,\mathrm{Pr}^{1/3}\sqrt{1+3.65\left(\mathrm{Re}_p^{*}\right)^{-1/2}}\right)^3} \right]^{-1/3} \quad (4)$$

where, $\mathrm{Pr} = \mu_a C_{p,a} / k_a$ is the Prandtl number. μ_a, $c_{p,a}$ and k_a are the dynamic viscosity, specific heat capacity at constant pressure, and thermal conductivity of air, respectively. It is noted that this correlation is valid in the range $0.1 < \mathrm{Re}_p^{*} < 100$ where $\mathrm{Re}_p^{*} = \mathrm{Re}\, pL^{-1}$ is the modified spacing channel Reynolds number. $\mathrm{Re} = \rho_a v_{ch} D_h / \mu_a$ is the internal flow Reynolds number with ρ_a being the density of air, v_{ch} being the air velocity through the fin channels and $D_h=2p$ being the hydraulic diameter of the channel. The efficiency of the fin (η) can be calculated as [42]:

$$\eta = \frac{\tanh\sqrt{2Nuk_a H^2 (t+L)/(kptL)}}{\sqrt{2Nuk_a H^2 (t+L)/(kptL)}} \quad (5)$$

where, k is the thermal conductivity of the heat sink material. The heat transfer coefficient can be estimated from the Nusselt number as $h = Nuk_a / p$. The overall fin to ambient heat transfer resistance can therefore be estimated as:

$$R_{sa} = \frac{1}{\eta h A_{hs,\,fin}} + \frac{1}{h A_{hs,b}} \tag{6}$$

where, $A_{hs,fin}$ is the total finned surface area and $A_{hs,b}$ is the total base area not covered by fins.

Since the heat source and the substrate dimensions do not match, there will be an additional resistance associated with the spreading of heat. Since VAM calculates the spreading resistance of a layer using the thermal conductivity of the subsequent layer below it as the boundary condition, it cannot be used to accurately predict the spreading resistance of the final layer (heat sink). The spreading resistance (R_{spr}) for the heat sink can thus be evaluated using the following correlation [43]:

$$R_{spr} = \frac{1}{2}\frac{(1-\varepsilon)^{3/2}}{k\sqrt{A_s}}\frac{\tanh(\lambda\tau) + \frac{\lambda}{Bi}}{1 + \frac{\lambda}{Bi}\tanh(\lambda\tau)} \tag{7}$$

Where, $\varepsilon = r_s/r_b$ and $\tau = t_b/r_b$ are the dimensionless contact radius and plate thickness with $r_s = \sqrt{A_s/\pi}$ and $r_b = \sqrt{A_b/\pi}$ being the equivalent radii of the heat source and the baseplate having cross-sectional areas A_s and A_b respectively. $\lambda = \pi + \left(\sqrt{\pi}\varepsilon\right)^{-1}$ is an empirical parameter, and $Bi = hr_b/k$ is the dimensionless Biot number, which captures the effect of different cooling conditions at the heat sink surface on the spreading resistance. Finally, the conductive resistance (R_c) for the thickness t_b can be estimated as:

$$R_c = \frac{t_b}{kA_s} \tag{8}$$

The total heat sink resistance is now estimated as:

$$R = R_c + R_{spr} + R_{sa} \tag{9}$$

A copper heat sink described in Figure 4 and detailed in Table 3 is considered as the baseline in this study. To estimate the influence of high thermal conductivity polymers,

the performance of a polymeric heat sink with dimensions identical to the baseline heat sink was also modeled. The thermal conductivity of the polymer was assumed to be 20 W/mK; it is noted that polymer nanocomposites with such high values of thermal conductivity have been synthesized.

Furthermore, the thermal benefits of dual-side air cooling [44] were also estimated. In the present embodiment of dual-side cooling, heat is rejected via a polymeric heat sink attached to a baseplate and one mounted on top of the chip.

2.2.2 Indirect liquid cooling (single-phase) (coolant: water)

While air cooling has significant advantages in terms of simplicity, low heat transfer coefficients restrict the suitability of air cooling for high heat flux packages. Single-phase liquid cooling techniques employing microchannel heatsinks can handle much higher heat loads and have received significant research and development interest over the past two decades [45]–[47].

Presently, a microchannel heat sink with dimensions similar to those of the air-cooled sink is considered, as illustrated in Figure 5.

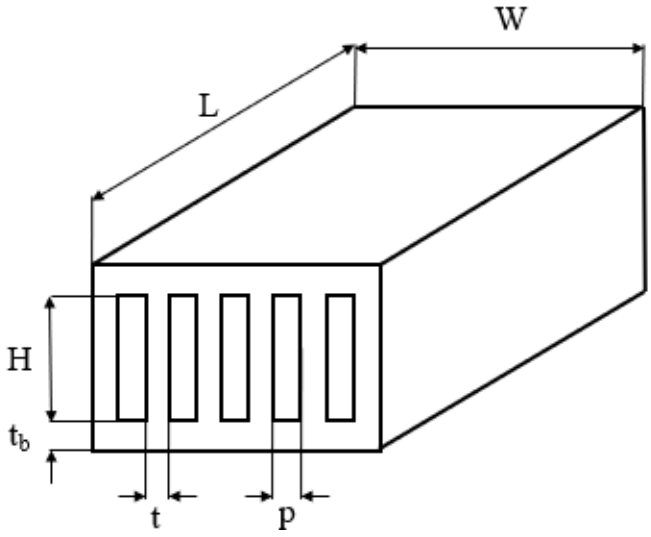

Figure 5. Schematic of the microchannel heat sink employed in the present study.

The correlation proposed by Muzychka and Yovanovich [48] is used to evaluate the heat transfer coefficient where the Nusselt number is estimated as:

$$Nu_{\sqrt{A}} = 3.24\left(\frac{f\,\mathrm{Re}_{\sqrt{A}}}{8\sqrt{\pi}\varepsilon^{0.1}}\right) \tag{10}$$

where, f is the friction factor given by:

$$f\,\mathrm{Re}_{\sqrt{A}} = \frac{12}{\sqrt{\varepsilon}\left(1+\varepsilon\right)\left[1-\frac{192\varepsilon}{\pi^5}\tanh\left(\frac{\pi}{2\varepsilon}\right)\right]} \tag{11}$$

where, ε is the aspect ratio of the microchannel and Reynolds number is based on the square root of the cross-sectional area.

The equations to predict conductive, sink to ambient resistance, and the spreading resistance remain unchanged. However, they have to be evaluated using the value of the heat transfer coefficient estimated from Equation 10. Furthermore, for internal flows, the caloric resistance (R_{cal}) comes into play due to the temperature gradient existing in the coolant along the flow direction. This caloric resistance can be estimated as [49]:

$$R_{cal} = \frac{1}{\rho Q c_p} \quad (12)$$

where, c_p is the specific heat capacity and Q is the volumetric flow rate of the coolant. The overall thermal resistance can then be estimated as:

$$R = R_c + R_{sa} + R_{spr} + R_{cal} \quad (13)$$

2.2.3 Direct liquid cooling (single phase) (coolant: water)

Direct liquid cooling replaces the conventional technique of dissipating heat using a heat sink connected to the baseplate. This technique obviates the need for a baseplate. The heat sink is directly connected to the direct bonded copper (DBC) substrate. The heat sink and hence the heat transfer coefficient remains identical as that for the indirect cooling case except for the spreading resistance which has to be reevaluated due to different dimensions of heat source originating from the DBC.

2.2.4 Two-phase cooling (coolant: R134a)

A drawback of single-phase microchannels is the temperature gradient in the fluid along the streamwise direction, which leads to a caloric thermal resistance (R_{cal}). Importantly, high caloric resistances imply high-temperature gradients in the device. Two-phase flow cooling works via latent heat exchange between the device and the coolant, which results in higher heat transfer coefficients compared to those achieved with sensible heat exchange. For well-designed systems, the coolant remains close to its saturation temperature throughout the cooling domain, which results in a more uniform temperature distribution throughout the device. The use of refrigerants for two-phase cooling has been widely studied. Presently, two-phase heat sinks are incorporated as an evaporator in a refrigeration cycle [50].

In order to calculate the two-phase flow microchannel heat sink resistance, the heat transfer coefficient was evaluated using the following saturated flow boiling heat transfer correlations [51]:

$$h_{cb} = \left[5.2\left(Bo\frac{P_H}{P_F} \right)^{0.08} We_{fo}^{-0.54} + 3.54\left(\frac{1}{X_{tt}} \right)^{0.94} \left(\frac{\rho_g}{\rho_f} \right)^{0.25} \right] \left(0.023 \mathrm{Re}_f^{0.8} \mathrm{Pr}_f^{0.4} \frac{k_f}{D_h} \right)$$

$$h_{nb} = \left[2345\left(Bo\frac{P_H}{P_F} \right)^{0.7} P_R^{0.38} \left(1-x\right)^{-0.51} \right] \left(0.023 \mathrm{Re}_f^{0.8} \mathrm{Pr}_f^{0.4} \frac{k_f}{D_h} \right) \quad (15)$$

$$h_{tp} = \left(h_{nb}^2 + h_{cb}^2 \right)^{0.5}$$

where, $Bo = q_H'' / Gh_{fg}$, $P_R = P / P_{crit}$, $\mathrm{Re}_f = G\left(1-x\right)D_h / \mu_f$, $We_{fo} = G^2 D_h / \rho_f \sigma$ $X_{tt} = \left(\mu_f / \mu_g \right)^{0.1} \left((1-x)/x \right) \left(\rho_g / \rho_f \right)^{0.5}$. Here subscripts *f* and *g* denote saturated fluid and gas respectively, *x* denotes thermodynamic equilibrium quality, q_H'' is the heat flux averaged over the heated perimeter of the channel, *G* is the mass velocity of the fluid and P_{crit} is the critical pressure. The properties of R134-a to evaluate the heat transfer coefficient were evaluated at a temperature of 10 ^{o}C. The conductive, spreading, and sink to ambient resistances were evaluated using Equations 6-8 respectively.

2.2.5 Jet impingement cooling (coolant: water)

The use of jet impingement cooling has been studied for front-end/ chip side cooling or back-side/baseplate or DBC cooling [52]. In the former case, the devices are typically coated with a dielectric layer, with the coolant impinging on the devices. The dielectric layer offers high thermal resistance despite its low thickness due to poor conductivity of typical dielectric materials. Front-end approaches also raise practical concerns related to the mechanical durability of the dielectric layer under the action of the impinging jets. Presently, a back-end approach was considered with microjets impinging

directly on the baseplate. It is noted that the impingement area can be modified so that the jets hit the hot spots on the baseplate. The heat transfer coefficient associated with jet impingement was estimated using [1] :

$$Nu = 0.5K_1 \,\mathrm{Re}^{0.67}\,\mathrm{Pr}^{0.42} \tag{16}$$

where,

$$\begin{aligned} K_1 &= K_2\left(1+\left(\left(H/D\right)K_3/0.6\right)^6\right)^{-0.05} \\ K_2 &= K_3\left(2-4.4K_3\right)/\left(1+0.2\left(H/D-6\right)K_3\right) \\ K_3 &= 0.886/\left(P/D\right) \end{aligned} \tag{17}$$

2.2.5 Spray cooling (coolant: water)

Spray cooling is another attractive option for ultrahigh heat flux dissipation. Spray cooling techniques use nozzles that atomize the coolant and spray it onto the hot surface at high pressure [53]. Atomization increases the surface area to volume ratio of the droplets and results in a more uniform spatial distribution of droplets on the heated surface. Furthermore, the high pressure of the impinging droplets helps overcome the opposing momentum of the Leidenfrost vapor film generated on high-temperature surfaces. This technique can be implemented directly on the chip or the baseplate (similar to the jet impingement). The heat transfer coefficient associated with spray cooling can be estimated using the single-phase heat transfer correlation for full cone pressure nozzles [54]:

$$Nu = 2.512\,\mathrm{Re}_s^{0.76}\,\mathrm{Pr}^{0.56} \tag{18}$$

where, Re_s is the spray Reynolds number, defined as $\mathrm{Re}_s = \rho Q'' d_{32}/\mu$, ρ is the fluid density, Q is the volumetric spray flux, d_{32} is the Sauter mean diameter (defined as the diameter of the droplet whose surface area to volume ratio is the same as that for the entire

spray sample) and μ is the dynamic viscosity of the fluid. *Nu* is the Nusselt number defined as $Nu = hd_{32} / k$, where *k* is the thermal conductivity of the coolant.

2.3 Results- Comparison of advanced cooling technologies

Figure 6 shows the thermal resistances of various layers of the IGBT package obtained using the variable angle model (VAM). It is evident that the alumina layer in the DBC has the maximum thermal resistance amongst all the layers due to its poor thermal conductivity (26 W/mK) compared to the other layers in the package. One way to decrease this resistance would be to substitute the alumina layer with high thermal conductivity ceramic materials such as Aluminum Nitride (AlN: k=140-180 W/mK) or decrease the thickness of the layer. Since the ceramic layer in the DBC serves to offer electrical insulation to the subsequent layers, there would be a limit on the minimum thickness below which the DBC would be susceptible to electrical failures.

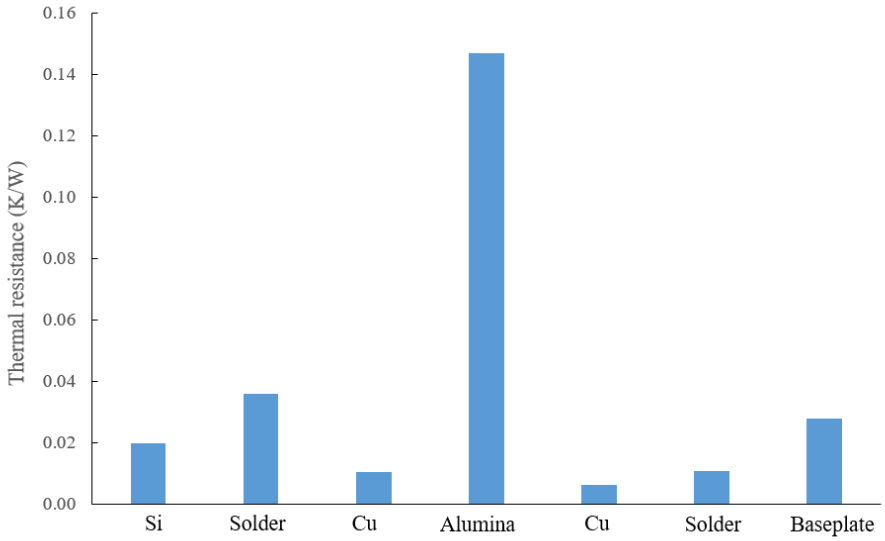

Figure 6. Comparison of thermal resistances of various layers of the IGBT package (using variable angle methodology (VAM)).

Figure 7 outlines the heat sink thermal resistances for copper (Cu) and polymeric heat sinks (k= 20 W/mK) evaluated for various cooling technologies. As expected, the thermal resistance is the lowest for a two-phase cooled Cu heat sink. This can be attributed to a very high heat transfer coefficient resulting from latent heat removal in two-phase cooling combined with the high thermal conductivity of the Cu material. The thermal resistances for the polymeric heat sinks are much higher compared to their Cu counterparts. The thermal conductivity influences the sink to ambient resistance via the fin efficiency term and thereby affects the thermal performance of the sink, with higher conductivities translating to higher fin efficiencies. While it is difficult to extract the physical significance of the thermal conductivity from the expression for the spreading resistance, it can be said that a higher thermal conductivity offers lesser resistance to in-plane lateral conduction and therefore lesser spreading resistance as is evident from Figure 7 with spreading resistances being much higher for polymeric heat sinks. Importantly, spreading resistance comprises a major chunk (43-71%) of the overall thermal resistance for polymeric heat sinks.

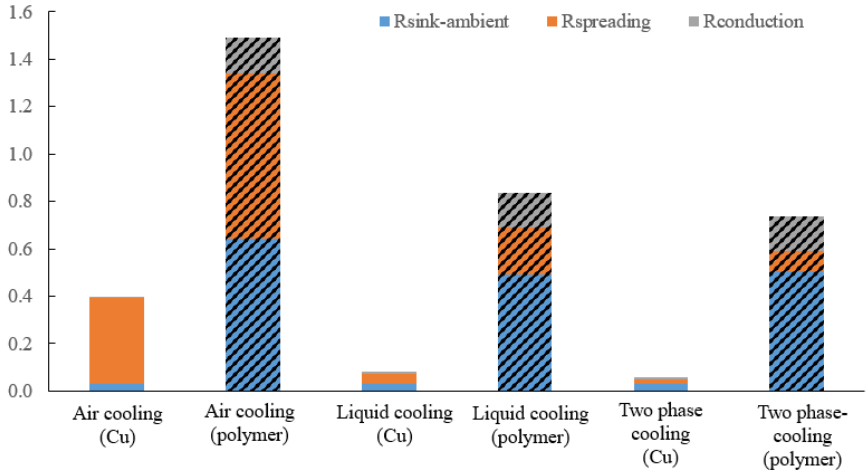

Figure 7. Estimated heat sink thermal resistances for various cooling technologies.

Since the thermal resistance of polymeric heat sink is high, one option to decrease the overall thermal resistance of the package would be to open thermally conductive

pathways in the vertical direction directly above the chip by resorting to a dual-sided cooling approach where an additional polymeric heat sink rests on top of the chip. Figure 8 illustrates the thermal resistance for a polymeric heat sink resting on top of the Si chip for different cooling technologies. While the sink to ambient and conductive resistances remains the same, the spreading resistance significantly increases due to a much smaller dimension of the heat source (chip as compared to the baseplate) thereby increasing the overall resistance of the heatsink.

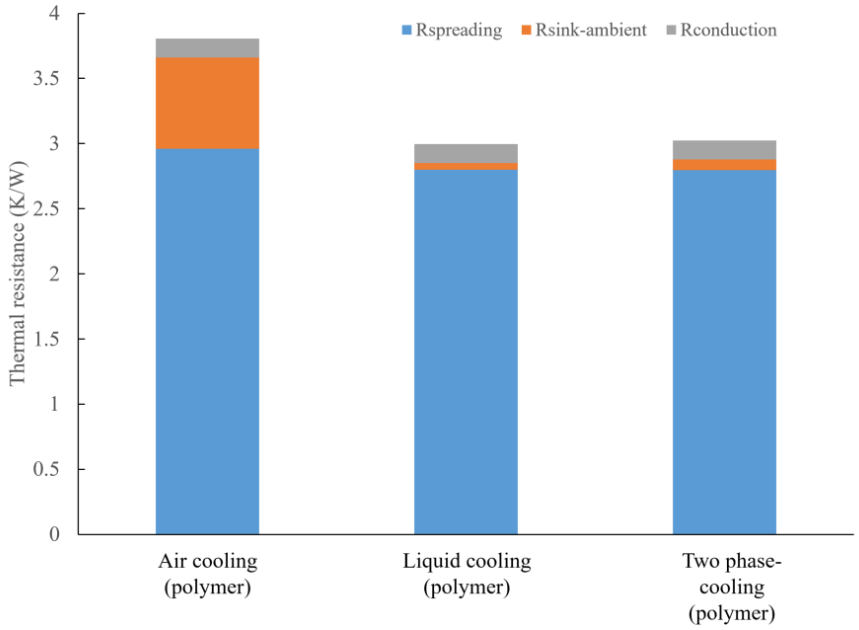

Figure 8. Thermal resistances for polymeric heat sinks (k=20 W/mK) on top of the chip.

Table 4 and Figure 9 summarize the maximum allowable heat flux for Si and SiC devices based on maximum allowable junction temperatures of 125 ^{o}C and 200 ^{o}C, respectively. Highlights and key takeaways can be summarized as:

1. Replacing a copper heat sink with a polymeric heat sink significantly decreases (3X reduction in maximum heat flux) the thermal performance for air and liquid (single

and two-phase) cooling. It is noted that the thermal conductivity of the polymer was assumed to be 20 W/mK, which is significantly higher than most existing polymers. Such high conductivities are only possible via the addition of high thermal conductivity filler materials into a base polymer. Significant materials development-related efforts are required to synthesize high thermal conductivity polymers, which also meet the mechanical and electric requirements of packaging.

2. Replacing an air-cooled copper heat sink with a polymer heat sink (k=20 W/mK) necessarily requires the use of single or two-phase liquid cooling to get comparable heat dissipation, albeit with a reduction in the thermal performance. The present analysis shows that polymers with high thermal conductivity can only be used in low heat dissipation packages (100-200 W/cm^2 for Si device packages and 200-380 W/cm^2 for SiC-based packages).
3. Replacing an air-cooled copper heat sink with a polymer heat sink (k=20 W/mK) will require dual-sided air cooling if the complexities associated with liquid cooling are to be avoided. However, the thermal performance would still be lower (0.55x) than that achievable by the baseline copper heat sink.
4. Water-cooled heat sink shows a significant improvement in thermal performance compared to the baseline air-cooled copper heat sink (2x enhancement in maximum heat flux dissipation compared to baseline). Furthermore, removing the baseplate and connecting the heat sink directly to the DBC results in a small reduction in the performance. This can be attributed to the higher thermal resistance associated with the spreading of heat in the heatsink which would have instead dissipated in the baseplate.
5. Two-phase cooling (R134A) shows superior thermal performance (24% enhancement for Cu heat sinks) when compared to single-phase water-based

cooling owing to high heat transfer coefficients associated with latent energy exchange.

6. The use of dual-sided cooling with polymer heat sinks (k=20 W/mK) results in a non-trivial increase in heat dissipation (~50 and 100 W/cm^2 for Si and SiC, respectively). It is noted that the spreading resistance will be significant for the heat sink placed on top of the chip (as illustrated in Figure 8) since the heat source dimensions (chip size) will be very small compared to the heat sink dimensions.
7. Jet impingement and spray cooling-based solutions display the highest levels of heat dissipation capability. It is noted that the heat transfer coefficient used for spray cooling has been derived for single-phase heat transfer; these values will be higher in the nucleate boiling regime.

It is noted that while these values were derived for a specific IGBT package, the key conclusions and trends reported in this study are expected to be applicable for other similar power electronics packages.

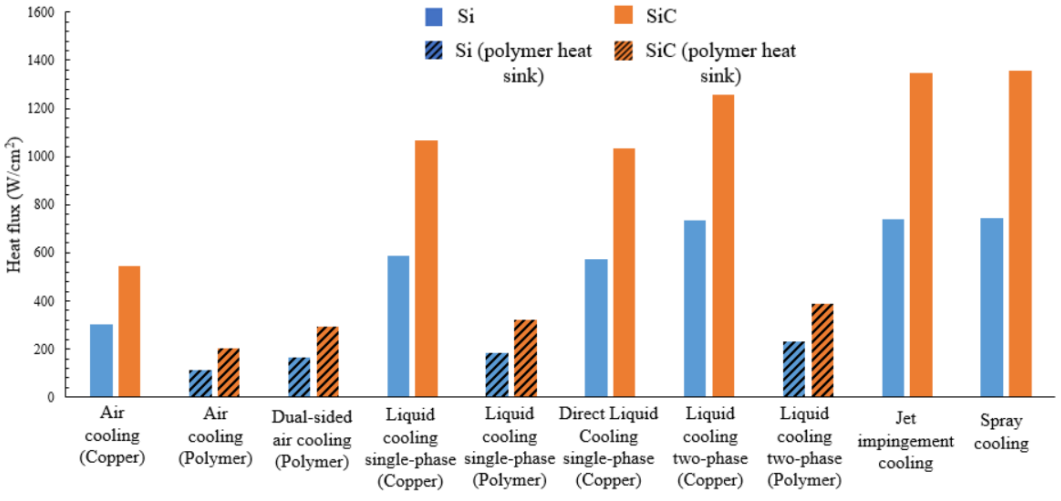

Figure 9. Impact of various cooling technologies on power electronics thermal management.

Table 4. Comparison of maximum allowable heat flux for different cooling technologies.

No.	Cooling technology	Coolant	Maximum allowable heat flux (W/cm^2)	
			Si (T_{jmax} =125 °C)	SiC (T_{jmax} =200 °C)
1	Baseline case: Air cooling (copper heat sink)	Air	304	543
2	Air cooling (Polymer heat sink; k= 20 W/mK)		115	202
3	Dual-sided cooling (polymer heat sinks)		167	292
4	Indirect liquid cooling: single-phase (copper heat sink)	Water	590	1067
5	Indirect liquid cooling: single-phase (polymer heat sink)		183	323
6	Direct liquid cooling: single-phase (copper heat sink)		572	1035
7	Liquid cooling: two-phase (copper heat sink)	R-134A	734	1259
8	Liquid cooling: two-phase cooling (polymer heat sink)		232	388
9	Jet impingement cooling	Water	738	1348
10	Spray cooling		742	1355
11	Dual-side liquid cooling single-phase (polymer heat sinks)		246	431
12	Dual-side liquid cooling: two-phase (polymer heat sinks)	R-134A	308	509

The thermal circuit and VAM-based model can also be used to predict the junction temperature for different levels of power dissipation. Table 5 outline the temperatures that will be experienced at Si junction for key cooling technologies employing copper as well as polymeric heat sinks at different levels of power dissipations. It is evident that the junction temperatures would be very high for polymeric heat sinks at both 100 and 200 W except for 2-phase cooling at low levels of power dissipation (<100). The key idea behind

this type of analysis is to obtain a first-order insight into the temperatures encountered at the junction of the package using different cooling technologies in conjunction with polymeric/copper-based heat sinks before.

Table 5. Junction temperature at various power dissipation levels for different cooling technologies.

No.	Cooling technology	Coolant	Junction temperature (ºC)	
			100 W	200 W
1	Baseline case: Air cooling (copper heat sink)	Air	90	156
2	Air cooling (Polymer heat sink; k= 20 W/mK)		199	374
3	Indirect liquid cooling: single-phase (copper heat sink)	Water	59	93
4	Indirect liquid cooling: single-phase (polymer heat sink)		134	243
5	Liquid cooling: two-phase (copper heat sink)	R-134A	41	72
6	Liquid cooling: two-phase cooling (polymer heat sink)		109	208
7	Jet impingement cooling	Water	52	79
8	Spray cooling		51	79

CHAPTER 3: FINITE ELEMENT ANALYSIS (FEA) SIMULATION OF INTEGRATED GATE BIPOLAR TRANSISTOR (IGBT) MODULE

This chapter details two types of FEA simulations carried out in ANSYS to quantify the benefits of using polymers as heat sinks and encapsulation materials. The first part of this chapter provides a direct comparison between variable angle methodology (VAM) and 3D FEA simulations as tools for estimating the thermal performance of an electronic package. In these simulations, the junction temperature of an IGBT package is estimated at two levels of power dissipation for different cooling technologies as outlined in Chapter 2. The second part of this chapter outlines a brief preliminary effort to understand the temperature distributions in a package as a function of the thermal conductivity of the encapsulant. Coupled 2-D electro-thermal simulations are carried out to evaluate the temperature distributions in the package with polymeric encapsulants of varying thermal conductivities covering the top of the Si chip.

3.1 3D FEA simulations for polymeric heat sinks

In order to carry out FEA simulations in ANSYS, a 3D model of the Semikron IGBT package was generated in Solidworks using the dimensions of the package and heat sink, as outlined in Table 4 and Table 5**.** The resulting model, illustrated in Figure 10, was then imported into the ANSYS environment.

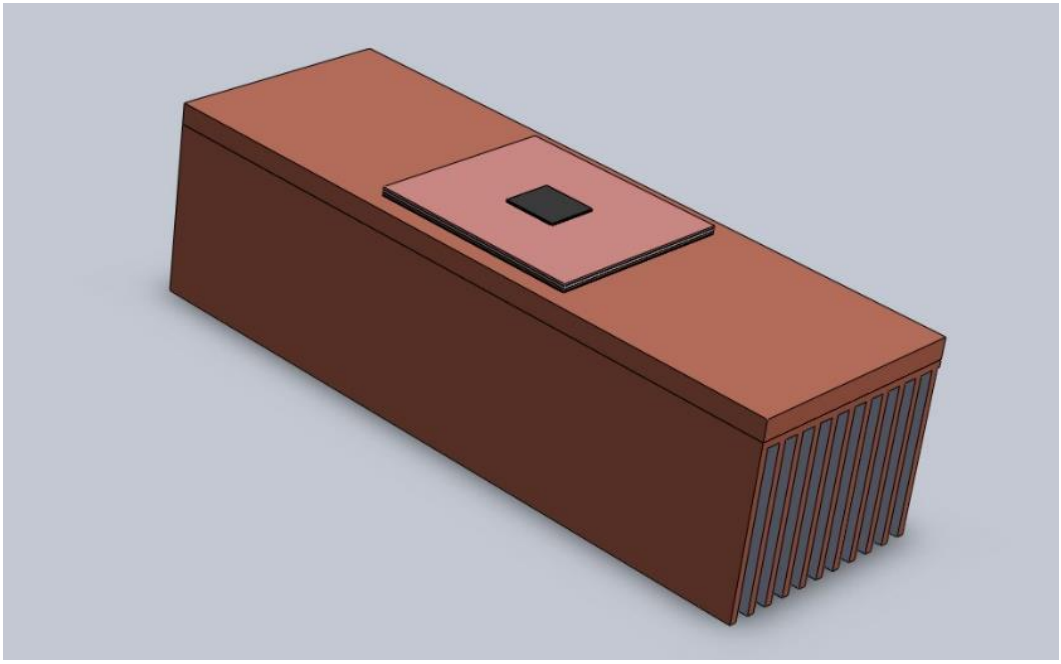

Figure 10. 3D model of the IGBT package used for the FEA simulations.

In order to set up the simulation environment, thermal conductivities, as outlined in Table 2, were assigned to individual layers of the IGBT package. Following this, the model was then meshed in ANSYS taking into account the relative dimensions of the IGBT layers. Since the heat sink and baseplate were relatively larger in dimension, a coarser mesh was utilized as compared to the meshes for the IGBT layers, wherein a fine mesh had to be used for improved resolution and reasonable computational times. Additionally, a mesh-independence study with different mesh sizes was carried out to confirm the robustness of the simulation results, and an optimal mesh size was used for final computations. A schematic showing the meshed package is outlined in Figure 11.

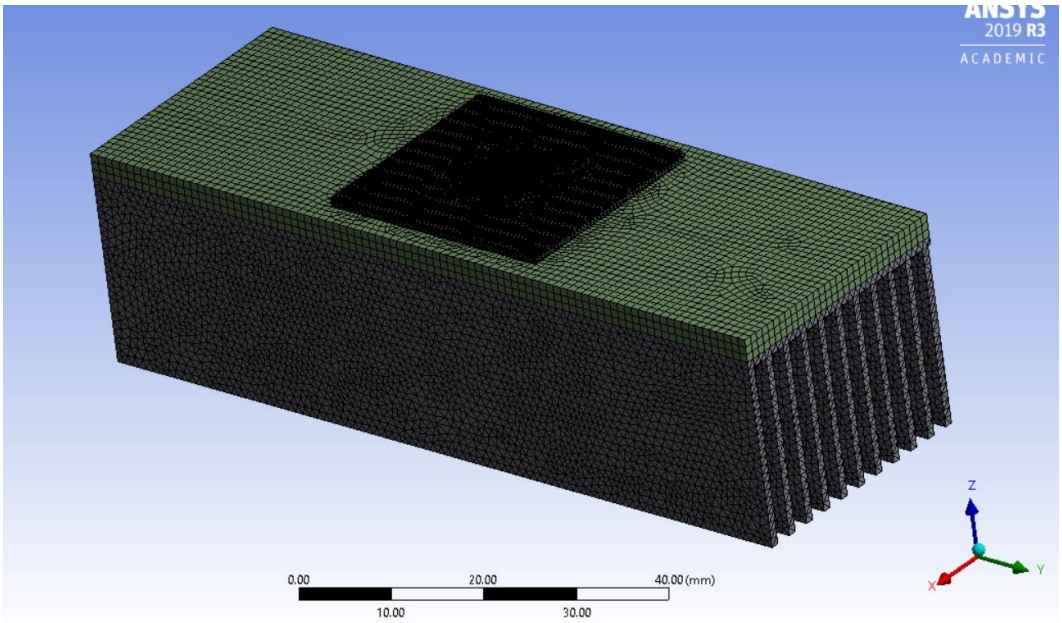

Figure 11. Meshed model of the IGBT package.

The boundary conditions for the simulations are illustrated in Figure 12 and are as follows: a heat source of 100/200 W at the top of the chip, and adiabatic conditions for the external surfaces of the package. The heat transfer coefficient at the internal surface of the heat sink was estimated using correlations outlined in Chapter 2 and are applied on a case-to-case basis based on the cooling technology employed.

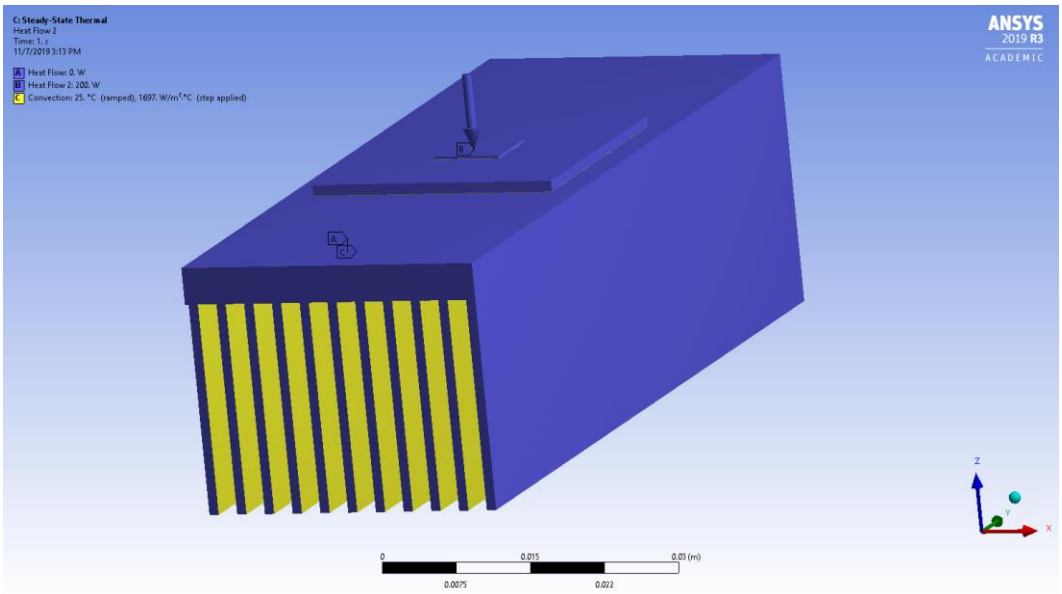

Figure 12. Boundary conditions for the FEA model. Heat transfer coefficients are evaluated using correlations and are applied either on the heat sink (air and liquid-cooled) or the baseplate (jet and spray impingement), based on the cooling technology utilized.

Figure 13 and Figure 14 show the temperature field resulting in the package connected to an air-cooled heat sink for the case when polymer (k=20 W/mK) and copper (k=400 W/mK) are used as heat sink materials for 100 W power dissipation. It is evident that heat is more uniformly dissipated due to higher thermal conductivity of the copper heat sink thereby resulting in lower junction temperatures. The non-uniformity of heat dissipation due to lower thermal conductivity is clearer in the heat sink temperature distribution (Figure 14) for a polymeric heat sink. The highest and lowest temperatures are 128 ^{o}C and 38 ^{o}C, respectively, whereas the highest and lowest temperatures for the copper heat sink was 69 ^{o}C and 51 ^{o}C respectively. Similar observations hold for a liquid-cooled sink as well (Figures 15 and 16), in addition to lower temperatures everywhere due to better heat removal (higher heat transfer coefficients) associated with liquid cooling.

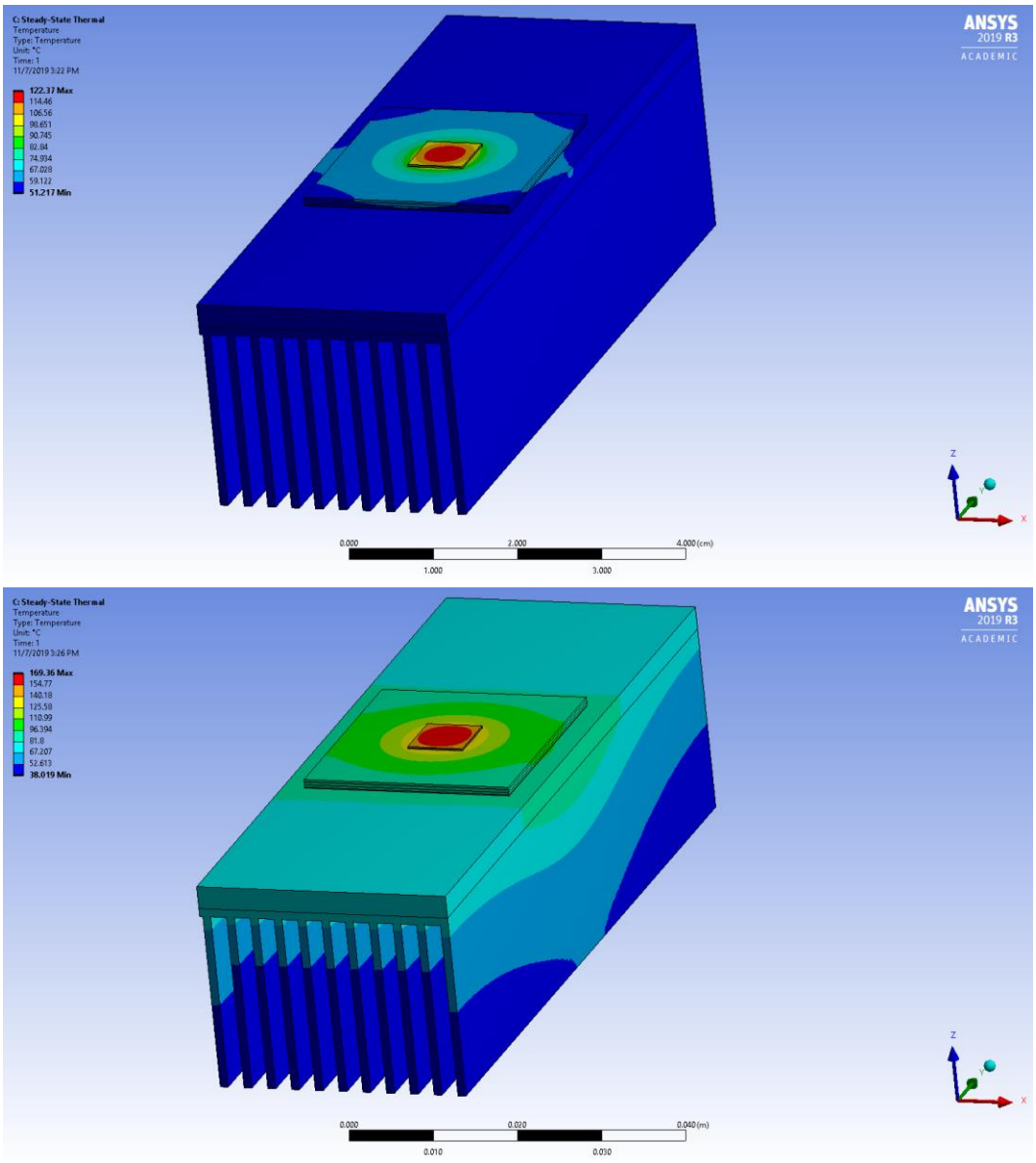

Figure 13. Temperature distribution in an IGBT package, coupled with an air-cooled heat sink made out of copper (top) and polymer with k=20 W/mK (bottom).

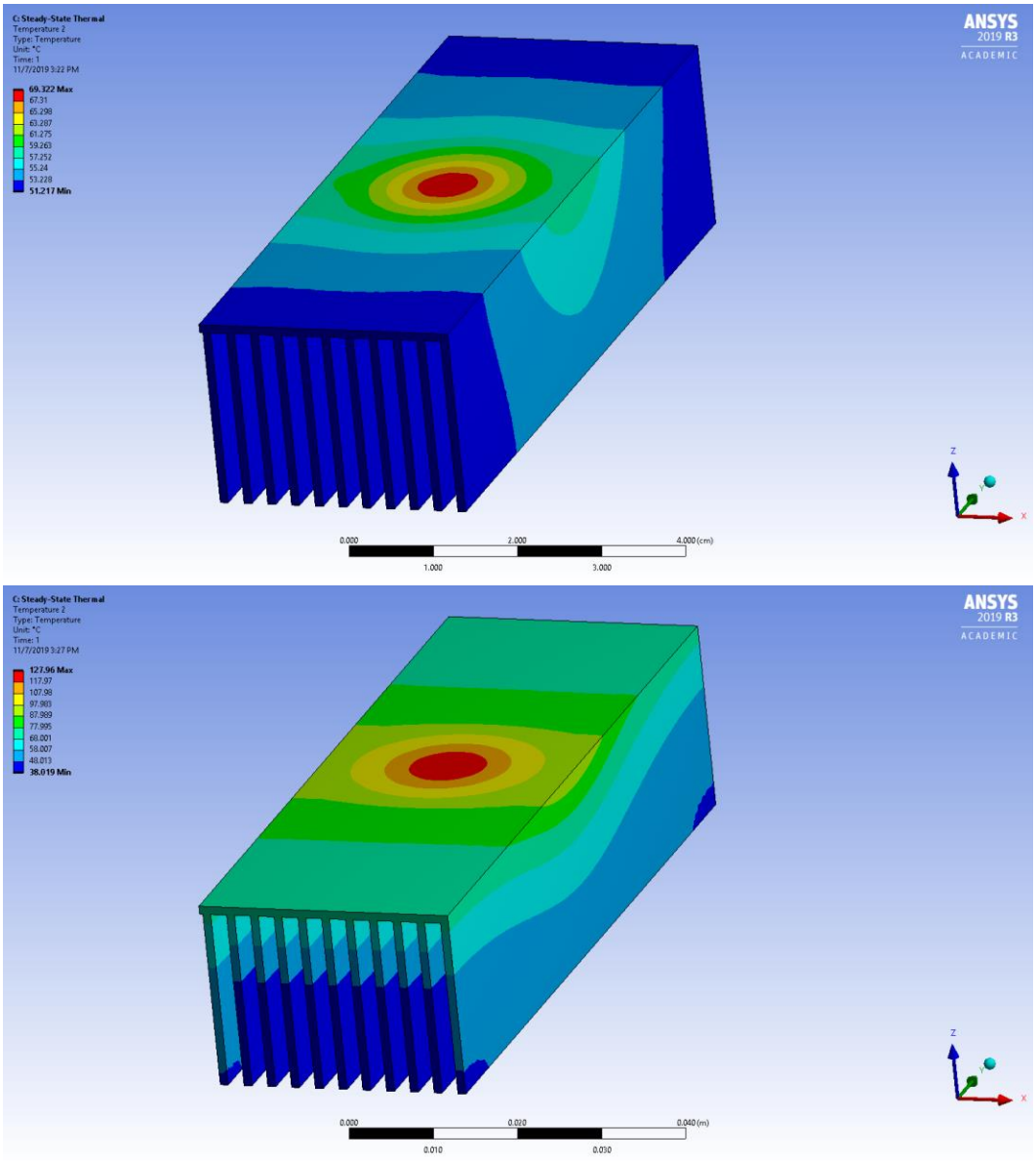

Figure 14. Temperature distribution in an air-cooled heat sink made out of copper (top) and polymer with k=20 W/mK (bottom).

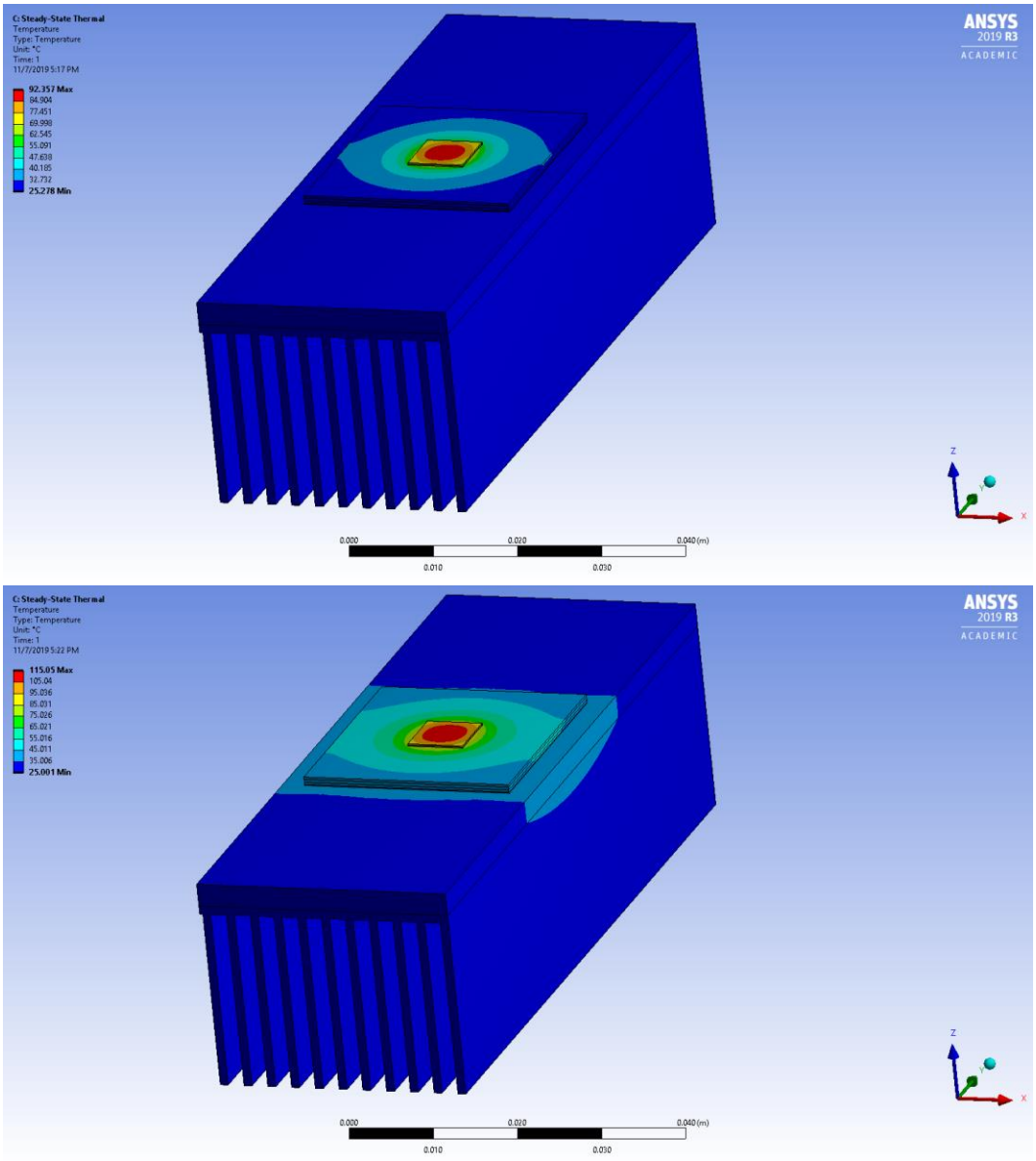

Figure 15. Temperature distribution in an IGBT package when coupled with a liquid-cooled heat sink made of copper (top) and polymer with k=20 W/mK (bottom).

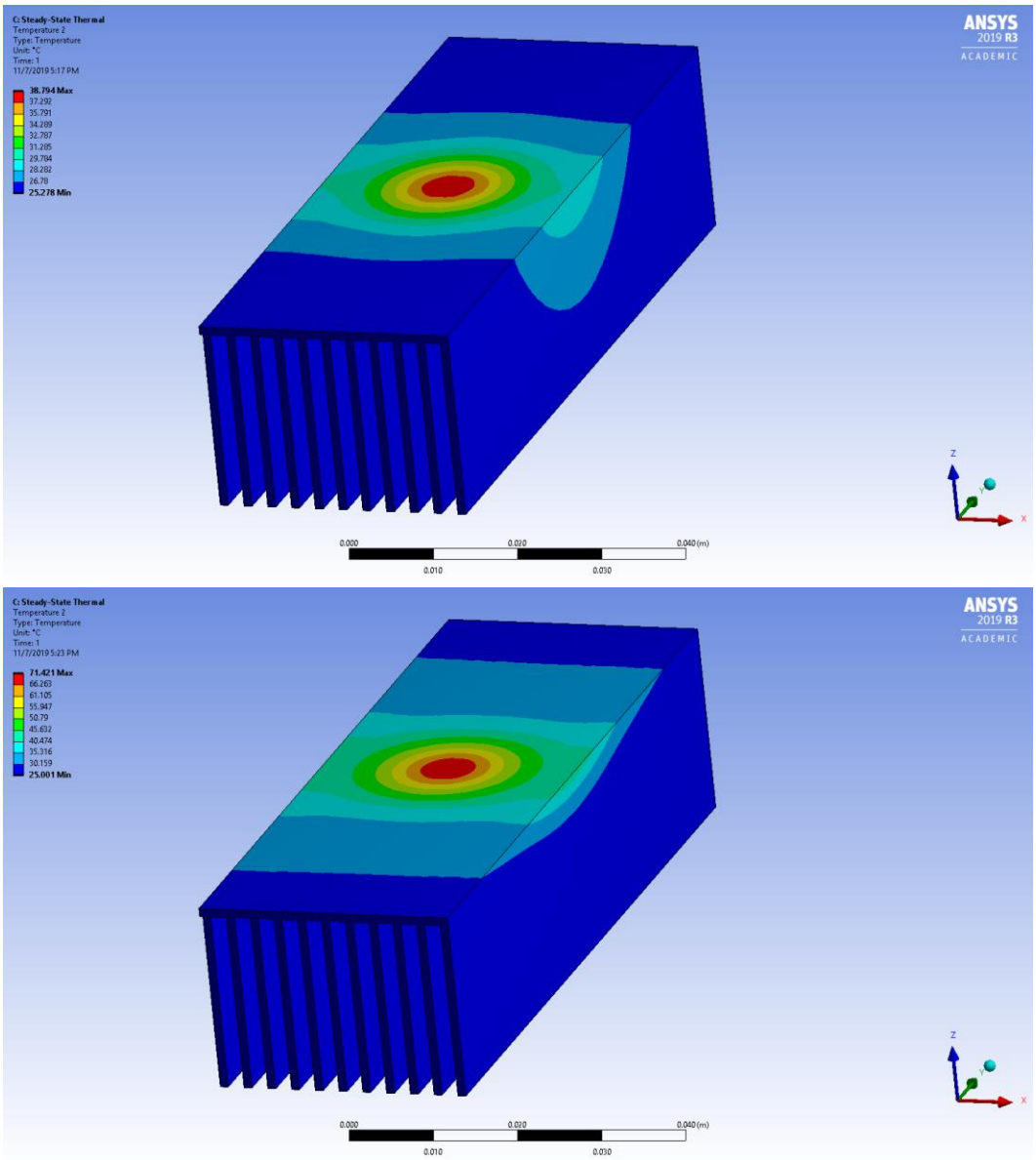

Figure 16. Temperature distribution in a liquid-cooled heat sink made of copper (top) and polymer with k=20 W/mK (bottom).

Table 6 is a comparison of the junction temperatures obtained via variable angle methodology and the present 3D FEA simulations with the error percentage relative to the FEA simulations mentioned in brackets. It is seen that the variable angle methodology, does not agree very well with the FEA simulations and can predict the junction

temperatures within an accuracy of 35% in most cases. The deviation from the FEA simulations inherently stems due to the approximations taken into consideration while deriving the variable angle model [38]. It is clear that VAM should only be used as a first-order tool to evaluate the thermal performance of a package or to decide and compare cooling technologies to be employed before resorting to time-consuming FEA simulations.

Table 6. Junction temperatures evaluated using VAM and FEA simulations.

No.	Cooling technology	Coolant	Junction temperature (ºC)			
			100 W		200 W	
			VAM	FEA	VAM	FEA
1	Baseline case: Air cooling (copper heat sink)	Air	91 (-18%)	111	156 (-21%)	197
2	Air cooling (Polymer heat sink; k= 20 W/mK)		199 (+27%)	157	374 (+29%)	289
3	Indirect liquid cooling: single – phase (copper heat sink)	Water	59 (-27%)	81	93 (-32%)	137
4	Indirect liquid cooling: single - phase (polymer heat sink)		134 (+30%)	103	243 (+35%)	181
5	Liquid cooling: two-phase (copper heat sink)	R-134A	41 (-33%)	62	73 (-36%)	113
6	Liquid cooling: two-phase cooling (polymer heat sink)		109 (+47%)	74	208 (+50%)	139
7	Jet impingement cooling	Water	52 (-30%)	75	79 (-37%)	125
8	Spray cooling		51 (-34%)	79	79 (-41%)	133

3.2 2D electro-thermal simulations to quantify benefits of polymeric encapsulants

The benefits of polymeric heat sinks on the thermal performance of an IGBT package has been studied using variable angle methodology and ANSYS simulations. It is important to note that all the analyses carried out so far considered only the downward path for the removal of heat, and the shortest path for heat transfer (chip to ambient temperature) from the top of the package was not considered. In reality, there will be very little heat transfer from the top, since most of the state of the art polymeric encapsulation materials comprising a majority of the space on top of the chip have a very poor thermal conductivity (~2 W/mK) and effectively act as insulators. However, using a polymeric encapsulant with a higher thermal conductivity can potentially open up thermally conducting pathways in the upward direction, thereby alleviating temperature spikes in the junction. High thermal conductivities can be achieved via the use of high thermal conductivity fillers such as boron nitride (h-BN), aluminum nitride (AlN), metallic nanoparticles, etc. interspersed in the polymer matrix [9]. The benefits of incorporating high thermal conductivity filler particles on the thermal conductivity of the polymer have been summarized in Table 1. It is important to note that such filler particles, in addition to enhancing the thermal conductivity also influence the mechanical and electrical properties of the nanocomposite.

Presently, simulations were conducted to assess the impact of improved thermal conductivity of polymers on the temperature distribution at a wire bond junction, which is surrounded by an encapsulant. 2-D steady, coupled electro-thermal simulations were carried out in ANSYS. The dimensions of the IGBT package remain the same as used in the previous section, with the exception of a bond wire and a polymeric encapsulant added on the top of the package. In terms of boundary conditions for the electrical analysis, a current of 25 A was passed through the wire with zero voltage applied to the copper plate

on top of the DBC substrate. For the thermal analysis, a constant temperature condition (25 ^{o}C) was applied to the bottom of the baseplate, and a convection coefficient of 5 W/m^{2}K was applied for stagnant air in contact with the exposed surface of the encapsulants, with the ambient temperature at 25 ^{o}C. All other external surfaces were considered to be adiabatic. Figure 17 illustrates the boundary conditions for the 2D FEA simulation. Simulations were carried out for heat sinks with two different thermal conductivities for the polymer (2 and 20 W/mK).

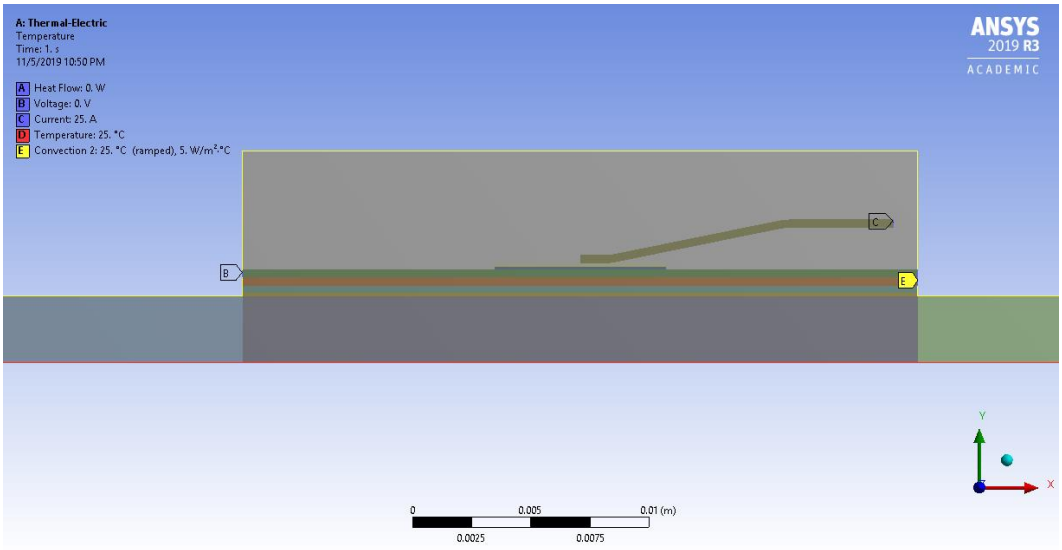

Figure 17. Boundary conditions for the 2D FEA simulation.

Figure 18 clearly illustrates the utility of opening up a thermally conducting pathway in the upward direction, where better heat dissipation is observed when polymers with higher thermal conductivities (>20 W/mK) are used as encapsulation materials. Lower temperatures are experienced at the junction with the use of high thermal conductivity polymeric encapsulants with the highest temperature being 78 and 71 ^{o}C for polymers with thermal conductivities 2 and 20 W/mK respectively. While hot spots and temperature gradients will always be present on the chip, it is seen that encapsulants with thermal

conductivities of O(10) W/mK, can result in meaningful reductions in hot spot temperatures and the resulting thermal gradients in the package.

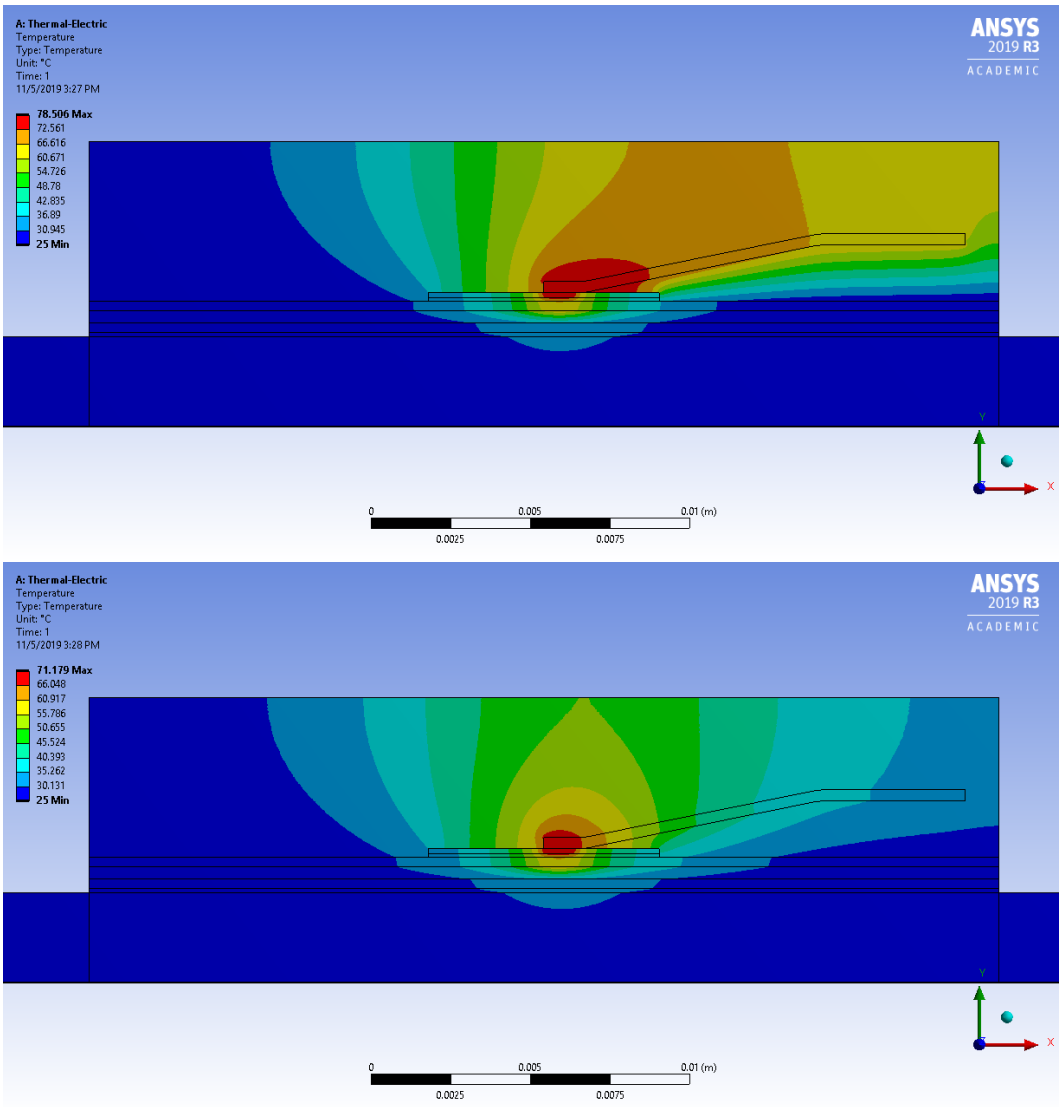

Figure 18. Temperature distribution resulting with a polymeric encapsulant of thermal conductivity 2 W/mK (top) and 20 W/mK (bottom).

CHAPTER 4: CONCLUSIONS

The emergence of wide bandgap materials, while attractive from the electrical standpoint brings along with it several challenges from the thermal perspective. It is important to assess multiple options for efficient thermal management of power electronics packages. In the present dissertation, the utility of using high thermal conductivity polymers as heat sinks (coupled with advanced cooling techniques) and as encapsulants has been studied. In doing so, specific polymers with high thermal conductivities, currently in the research phase were identified.

An analytical framework was developed to carry out a first-order assessment of the influence of polymeric heat sinks on the overall package thermal performance for Si and WBG-based devices. Multiple cooling technologies (air cooling, liquid cooling) were considered. It is seen that polymeric heat sinks with thermal conductivity of 20 W/mK can be used for low power dissipation packages (100-200 W/cm^2 for Si device packages and 200-380 W/cm^2 for SiC-based packages) when used in conjunction with advanced liquid cooling technologies. 3D FEA simulations demonstrate that the accuracy of the VAM tool is highly variable and it can only be used as preliminary evaluation tool to screen materials or cooling technologies for thermal management.

Preliminary simulations with the use of polymeric encapsulants show that polymers with thermal conductivities greater than 20 W/mK can open up thermally conductive pathways in the upward direction thereby alleviating the maximum junction temperature in the device. These findings should serve as motivation for future development of high thermal conductivity polymers, which also have optimized mechanical and electrical properties to increase overall package performance and reliability.

CHAPTER 5: FUTURE WORK

This dissertation presented a thermal resistance based framework to analyze the influence of various cooling technologies when used with polymeric heat sinks. Since transients are important in power electronics devices, the resistance circuit can be extended to include capacitances in the form of a Foster or a Cauer circuit. Variable angle model (VAM) can be used to calculate the capacitance of various layers of the IGBT package and the resulting network could be used to estimate the transient variation of temperatures in various layers of the package.

Dynamic thermal cycling generates thermo-mechanical stresses at the wire bond junctions, due to mismatch in the coefficient of thermal expansion (CTE) values of the materials at the interface. This often leads to wire bond failures and compromises package reliability. The 2-D simulations presented in the dissertation can be modified to include a cyclical current profile as the boundary condition. Additionally, they can be coupled with a mechanical environment to carry out 2D/3D transient electro-thermo-mechanical analysis. It is expected that high thermal conductivity polymeric encapsulants, in addition to alleviating the temperature spikes at the junction would also influence the interfacial stresses generated at the wire-bond chip interface; this will depend on the CTE and other thermo-mechanical properties of the encapsulant. Transient FEA simulations could be conducted to identify an optimum combination of thermal and mechanical properties, which increases the performance and overall lifetime of a power electronics package.

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